



Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 36246	SERIAL NO. 10/699,974
INFORMATION DISCLOSURE CITATION BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)		APPLICANT: Ian Zetterstrom Smith	
		FILING DATE: November 3, 2003	GROUP ART UNIT: 3724

U.S. PATENT DOCUMENTS

Examiner Initial		Document No.	Date	Name	Class	Subclass	Filing Date If Appropriate
	A						
	B						
	C						
	D						
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	J						
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FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Class	Subclass	Translation
	L	0 005 540	11/1979	European			English Abstract
	M	30 10 092 A1	09/1981	German			Cited on page 1 of the specification
	N	0 296 789	12/1988	European			English Abstract
	P						
	Q						

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

	R	
Examiner:		Date Considered: 11/16/05
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Form PTO-144

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
36246SERIAL NO.
10/699,974INFORMATION DISCLOSURE CITATION
BY APPLICANT
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Ian Zetterstrom SmithFILING DATE:
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U.S. PATENT DOCUMENTS

Examiner Initial		Document No.	Date	Name	Class	Subclass	Filing Date If Appropriate
JK	A	4,360,971	11/1982	Fellmann			
	B	4,364,435	12/1982	Tuggle et al.			
	C	2001/0034940 A1	11/2001	Marshall et al.			
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FOREIGN PATENT DOCUMENTS

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OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

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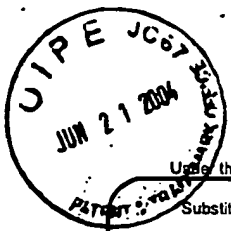
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PTO/SB/08A (08-03)

Approved for use through 07/31/2006. OMB 0651-0031

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1

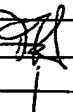
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Complete if Known

Application Number	10/699,974
Filing Date	11/02/2003
First Named Inventor	Isaiah O. Oladeji
Art Unit	2827
Examiner Name	
Attorney Docket Number	Jessen 12-4-6 (284)

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
[Signature]	1	US- 2001/0004550	06/21/2001	Passemard	
	2	US- 2003/0100190	05/29/2003	Cote et al.	
	3	US- 5,635,423	06/03/1997	Huang et al.	
	4	US- 5,821,169	10/13/1998	Nguyen et al.	
	5	US- 6,087,250	07/11/2000	Hyakutake	
	6	US- 6,143,646	11/07/2000	Wetzel	
	7	US- 6,150,073	11/21/2000	Huang	
	8	US- 6,156,643	12/05/2000	Chan et al.	
	9	US- 6,221,759	04/24/2001	Bothra et al.	
	10	US- 6,225,217	05/01/2001	Usami et al.	
	11	US- 6,255,735	07/03/2001	Wang et al.	
	12	US- 6,312,874	11/06/2001	Chan et al.	
	13	US- 6,468,898	10/22/2002	Usami	
	14	US- 6,479,391	11.12.2992	Morrow et al.	
	15	US- 6,507,081	01/14/2003	Smith et al.	
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FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear		T ⁶
		Country Code ³ *Number ⁴ *Kind Code ⁵ (if known)					
	16	WO 01/99184 A2	12/27/2001	Infineon Technologies			
	17	WO 01/43171 A1	06/14/2001	Infineon Technologies			

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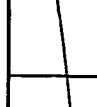
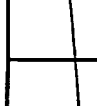
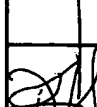
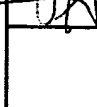
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	18	S. WOLF and R.N. TAUBER, Silicon Processing for VLS/Era, Volume 1 - Process Technology, pp. 797-799, Second Edition (2000) Published by Lattice Press, Sunset Beach, CA	
	19	VINCENT ARNAL et al., A Novel SiO ₂ -Air Gap Low K For Copper Dual Damascene Interconnect, Advanced Metalization Conference 2000, D. Edelstein et al., Warrendale, PA, USA, pp. 71-76	
	20	S. PURUSHOTHAMAN et al., Opportunities and Challenges in Ultra Low k Dielectrics for Interconnect Applications, IEEE, 2001, pp. IEDM 01-529-532	
	21	LYTLE et al., Overcoming Cu/CVD Low-k Integration Challenges in a High Performance Interconnect Technology, IEEE 2001, pp. IEDM 01-611-614.	
	22	ZIELINSKI et al., Damascene Integration of Copper and Ultra-Low-k Xerogel For High Performance Interconnects, 1997, pp. IEDM 97-936-938.	
	23	ARNAL et al., Integration of a 3 Level Cu-SiO ₂ Air Gap Interconnect for Sub 0.1 micron CMOS Technologies, 2001 IEEE, pp. 298-300.	

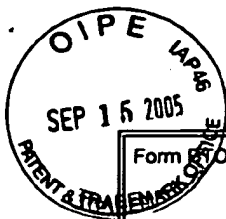
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U.S. PATENT DOCUMENTS

Examine r Initial		Document No.	Date	Name	Class	Subclas S	Filing Date If Appropriate.
<i>JK</i>	A	RE21,274	11/1939	J.A. Orr			1
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FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Clas s	Subclass	Translation
<i>JK</i>	L	747,292	04/1956	Great Britain			English Text
	M	0 005 540	11/1979	European			English Abstract
	N	0 296 789	12/1888	European			English Text
	P	0 976 313	12/1993	European			English Text
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OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

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